TIMER/TIMEOUT EVALUATION SYSTEM

ABSTRACT OF THE DISCLOSURE

An apparatus for evaluating at least one timer in the event of a timeout condition in a system includes circuitry that generates an indication that certain system conditions have occurred, clock circuitry, enabled by the indication, that generates a timeout counter enable signal, and a number of timer units, coupled to the clock circuitry, where each of the timer units is incremented an incrementing signal and reset by a monitored signal that represents conditions in the system. The apparatus includes comparison circuitry coupled to the timeout units, such that when at least one of the timer units reaches a predetermined count, the count, or the maximum count reached to this point, of each of the timer units is stored.